	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	73461	dram	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:14			0
2	BRS	16681	dram and (bit adj line)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/11 13:38			0
3	BRS	11541	dram and ((bit adj line) and (word adj line))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/11 13:45			0
4	BRS	0	dram and (architetecture)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/11 13:46			0
5	BRS	1051	(dram and ((bit adj line) and (word adj line))) and (LSI)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/11 13:47			0
6	BRS	133	((dram and ((bit adj line) and (word adj line))) and (LSI)) and (self adj alignment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/11 15:35			0
7	BRS	44	(((dram and ((bit adj line) and (word adj line))) and (LSI)) and (self adj alignment)) and (stacked adj capacitor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:20			0
8	IS&R	2	("5776815").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:38			0

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
9	IS&R	12	(("5206183") or ("5338700") or ("5488011") or ("5498562") or ("5500384") or ("5580011")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:42			0
10	IS&R	12	(("5206183") or ("5338700") or ("5488011") or ("5498562") or ("5500384") or ("5580811")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 09:51			0
11	IS&R	2	("5654236").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/06/12 10:19			0

L115 ANSWER 1 OF 2 WPIX (C) 2003 THOMSON DERWENT
AN 2002-530889 [57] WPIX
DNN N2002-420368 DNC C2002-150515
TI Method for the integration of DRAM memory by providing a cell architecture that augments the density of integration.
DC L03 U11 U14
IN CORONEL, P; LEVERD, F; PIAZZA, M
PA (SGSA) STMICROELECTRONICS SA
CYC 2
PI FR 2819633 A1 20020719 (200257)* 24p H01L021-8242
US 2002110976 A1 20020815 (200260) H01L021-8242
ADT FR 2819633 A1 **FR 2001-691 20010118**; US 2002110976 A1 US 2002-42520 20020108
PRAI **FR 2001-691 20010118**
IC ICM H01L021-8242
ICS H01L021-20; H01L021-4763
AB FR 2819633 A UPAB: 20020906
NOVELTY - A method for the integration of a Dynamic Random Access Memory (DRAM), allowing a freedom from the alignment margins inherent in the photoengraving of the upper electrode for the contact passage of the bit line, the retreat of the upper electrode being auto-aligned on the lower electrode, consists of:

(a) forming a topographical difference at the spot (A) where the opening for the upper electrode is to be realised;

(b) depositing a layer of non-doped polysilicon on the upper electrode;

(c) producing an implantation of strongly inclined doping in this layer;

(d) selectively engraving the non-doped part of the layer situated in the lower part of the zone (A) presenting the topographical difference;

(e) and engraving the remaining part of the polysilicon layer as well as the upper electrode layer situated in the lower part.

USE - The method is used for constructing an improved DRAM cell architecture to augment the density of integration.

ADVANTAGE - The method provides a cell architecture which improves the density of integration whilst retaining the same capacity produced by conventional methods whilst overcoming their lack of process robustness and limitations of productivity and cycle time.

DESCRIPTION OF DRAWING(S) - The drawing illustrates the DRAM cell architecture according to the invention.

Lower electrode layer; elec1
Upper electrode layer; elec2
Silicon oxide layers. TEOS

Dwg.9/9
FS CPI EPI
FA AB; GI
MC CPI: L03-G04A; L04-C11C
EPI: U11-C18B5; U14-C01